Compilation and Real-Time Analysis of a Synchronous Data-Flow Application on the Kalray MPPA Many-Core Processor

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Verimag (Grenoble INP)
Grenoble, France

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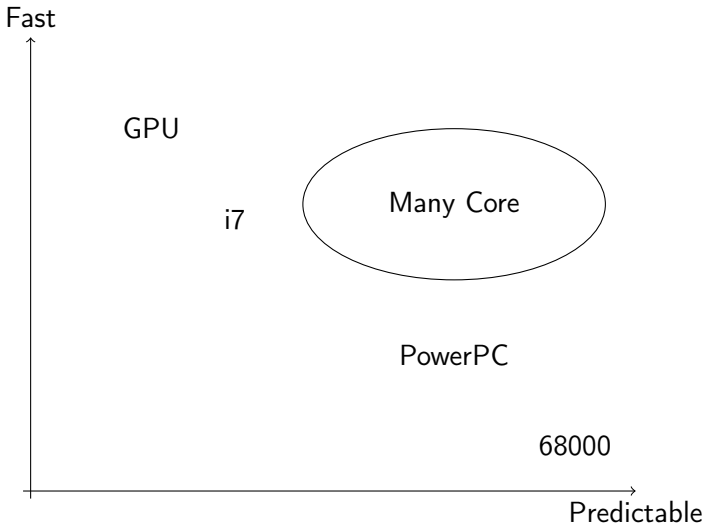
Outline

Outline

Time-critical, compute intensive applications

- Hard Real-Time: we must guarantee that task execution completes before deadline
- Compute-intensive
- Space/power bounded

Performance Vs Predictability



Many-core

=

Lots of simple cores

Many-core

=

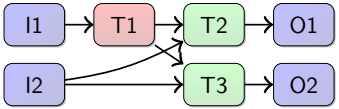
Lots of simple cores

Kalray MPPA (Massively Parallel Processor Array):

- 256 cores
- No cache consistency
- No out-of-order execution
- No branch prediction
- No timing anomaly

$\Rightarrow$ good fit for real-time?

Hard Real-Time on Many-Core



High-level Data-Flow Application Model

Synchronous hypothesis:
computation/communication in 0-time

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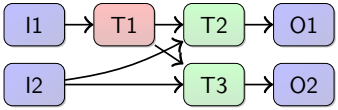

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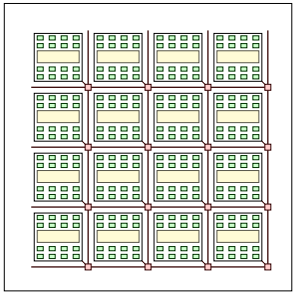

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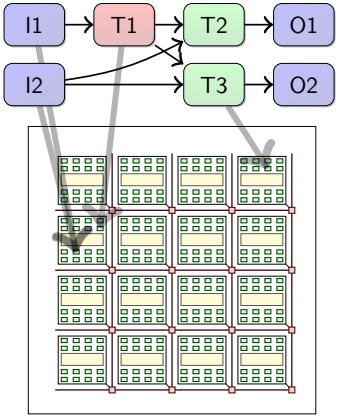

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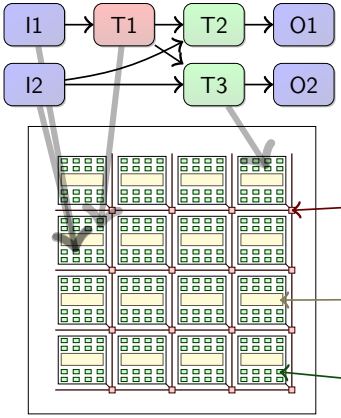

High-level Data-Flow Application Model

Synchronous hypothesis:
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Network On Chip

Communication takes time

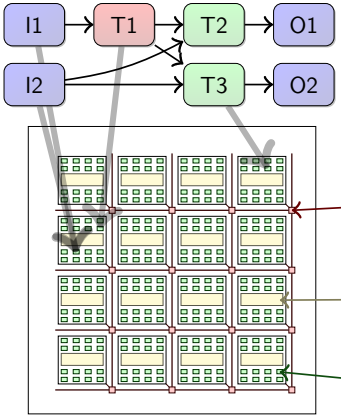
Shared Memory within Cluster

Interferences between tasks

Individual Cores

Cache, Pipeline, . . .

Hard Real-Time on Many-Core



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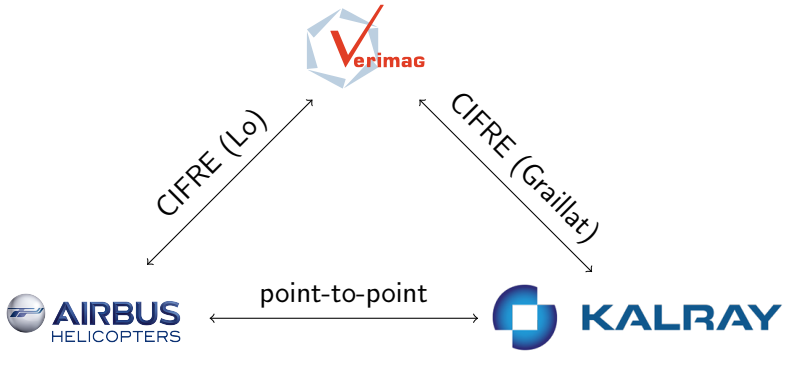
$\rightsquigarrow$ Take into account all levels
in Worst-Case Execution Time (WCET) analysis
and programming model

Context and Partners

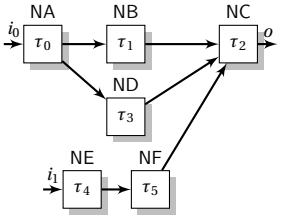


IRIT (WCET) IRISA (Scheduling) ONERA (NoC)

Projet CAPACITES (Ph.D Rihani)

Outline

Execution of Synchronous Data Flow Programs



High level representation

Single-core

code generation

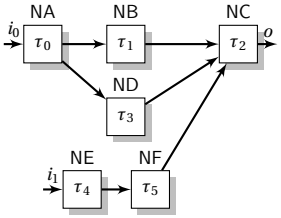
static non-preemptive scheduling

```
int main_app(i1, i2)
{
    na = NA(i1);
    ne = NE(i2);
    nb = NB(na);
    nd = ND(na);
    nf = NF(ne);
    o = NC(nb,nd,nf);
    return o;
}
```

Industrialized as SCADE (1993)

heavily used in avionics and nuclear

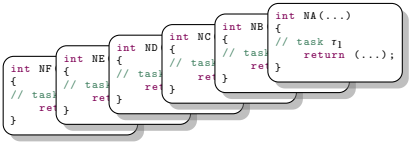
Execution of Synchronous Data Flow Programs



High level representation

Multi/Many-core

code generation



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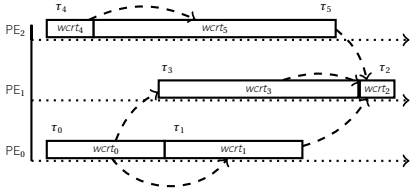

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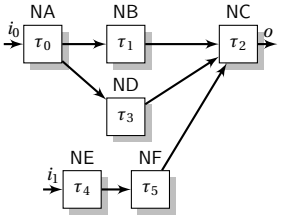

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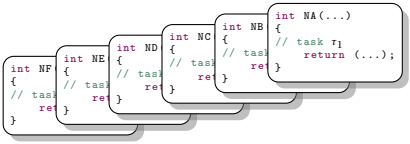
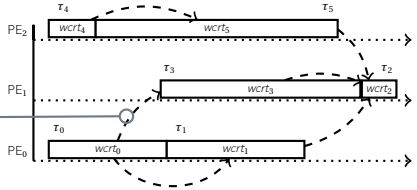


static non-preemptive scheduling

✓ Respect the dependency constraints



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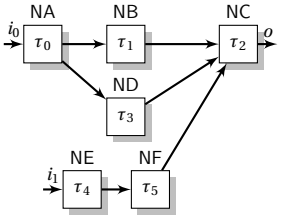

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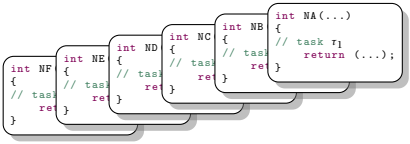

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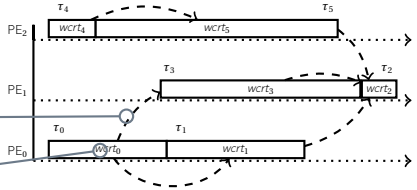
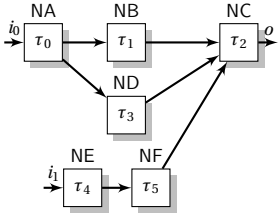
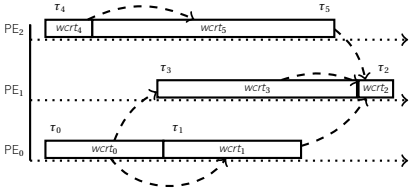


✓ Respect the dependency constraints

✓ Set the release dates to get precise upper bounds on the interference

Parallel code generation from Lustre/SCADE (pseudo-code)



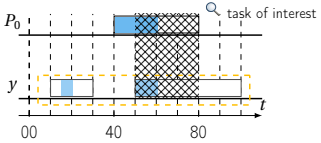



```
// Generated by SCADE KCG
void NA(ctx_a *ctx) {
    // ... computation ...
}

void NA_wrapper(ctx_a *ctx) {
    RECV_NA(i0);
    NA(ctx);
    SEND_NA_NB(...);
}
```

```
// Generated by us
void worker_PE0(void) {
    ctx_a ctxa; ctx_b ctxb;
    while (1) {
        NA_wrapper(&ctxa);
        wait(release_t2);
        NB_wrapper(&ctxb);
        wait(end_of_period);
    }
}

#define RECV_NA(data) ...
```

Contributions (part of Ph.D Hamza Rihani, with Claire Maiza)

1. Precise accounting for interference on shared resources in a many-core processor



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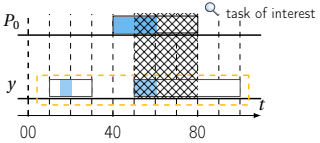
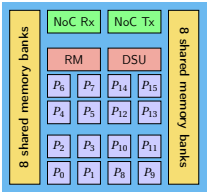


2. Model of a multi-level arbiter to the shared memory



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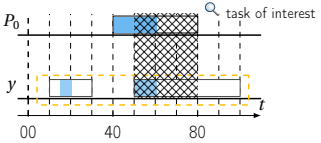

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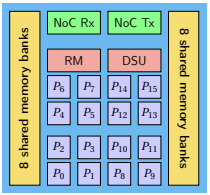
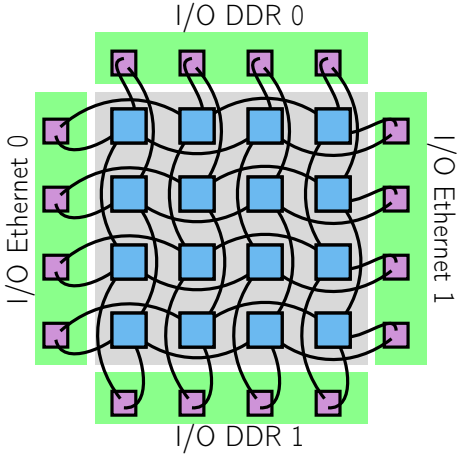


3. Response time and release dates analysis respecting dependencies.

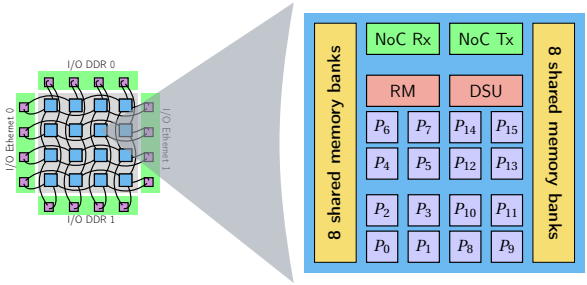
Outline

Architecture Model



- Kalray MPPA 256 Bostan
- 16 compute clusters + 4 I/O clusters
- Dual NoC (Network on Chip)

Architecture Model



Per cluster:

- 16 cores + 1 Resource Manager
- NoC Tx, NoC Rx, Debug Unit
- 16 shared memory banks (total size: 2 MB)

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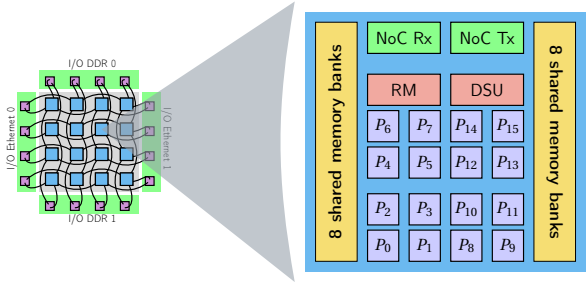

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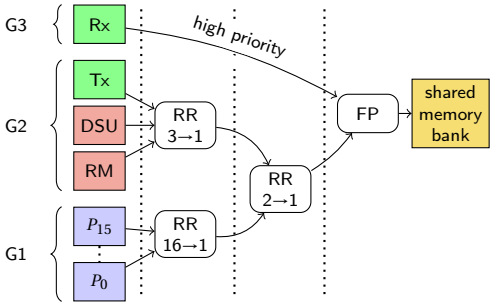
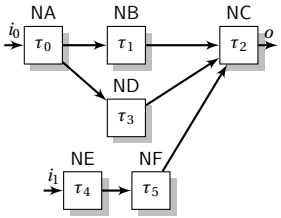
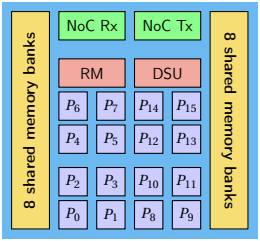
- Multi-level bus arbiter per memory bank



Execution Model





- Tasks mapping on cores
- Static non-preemptive scheduling
- Spatial Isolation

  different tasks go to different memory banks
- Interference from communications

- Execution model:
  - execute in a “local” bank
  - write to a “remote” bank

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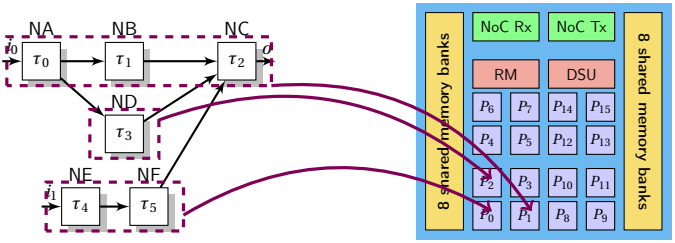

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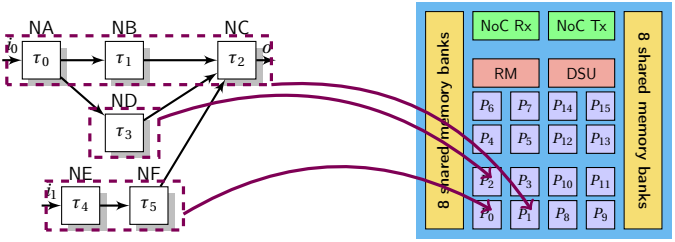

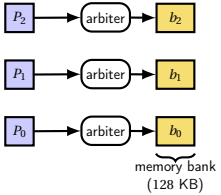

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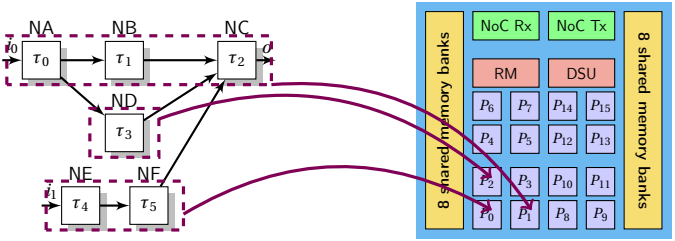

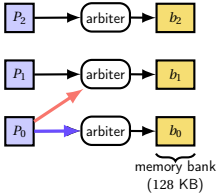

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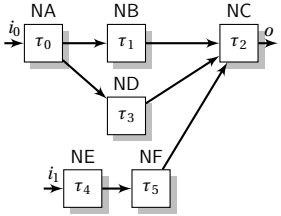

- Directed Acyclic Task Graph
- Mono-rate
- Fixed mapping and execution order

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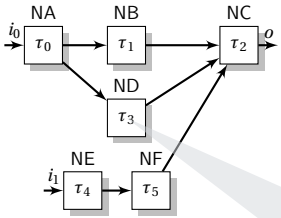

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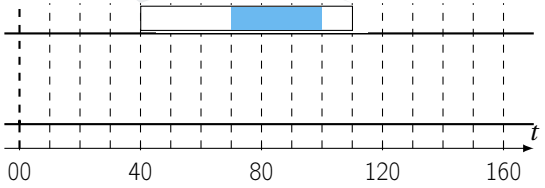

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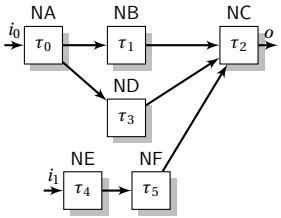

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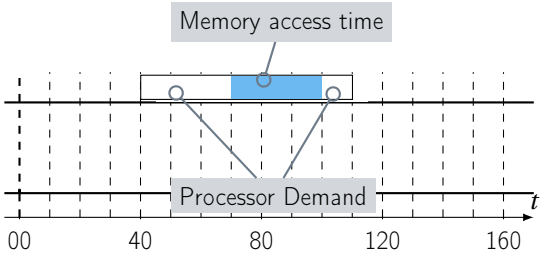

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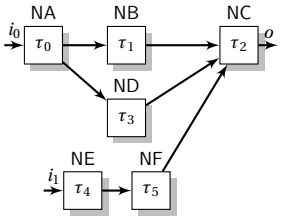

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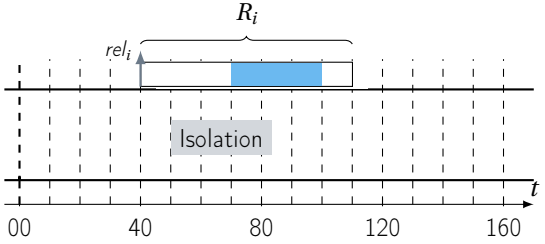

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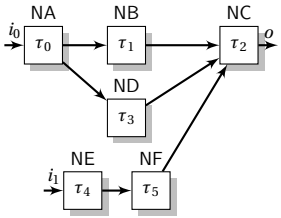

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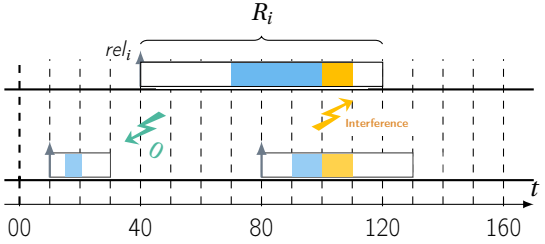

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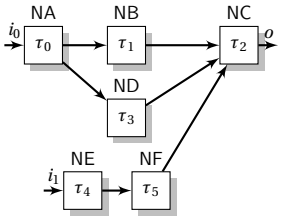

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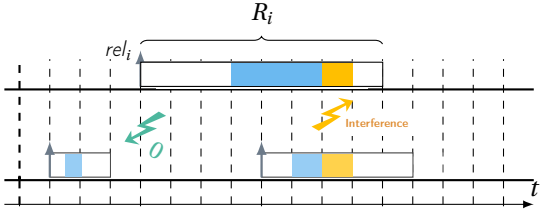

🔍 Find R_i (including the interference)
🔍 Find rel_i respecting precedence constraints

Outline

Response Time Analysis

$$R = PD + I^{BUS}(R)$$

- Response Time

Response Time Analysis

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- Response Time
  - Processor Demand

Response Time Analysis

$$R = PD + I^{BUS}(R)$$

- Response Time
  - Processor Demand
    - Bus Interference

(given a model of the bus arbiter)

Response Time Analysis

$$R = PD + I^{BUS}(R) + I^{PROC}(R) + I^{DRAM}(R)$$

- Response Time
  - Processor Demand
    - Bus Interference

(given a model of the bus arbiter)

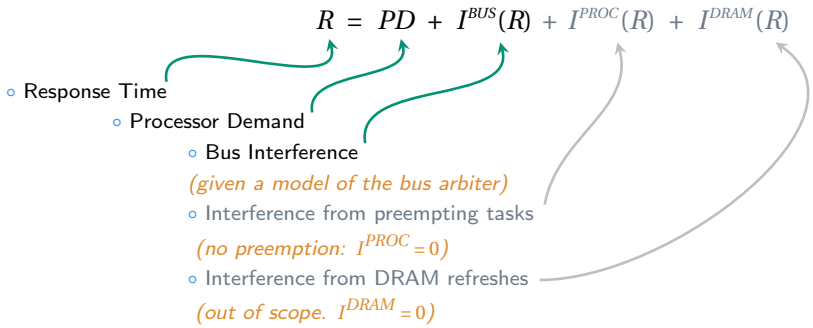
- Interference from preempting tasks

(no preemption: $I^{PROC} = 0$)

- Interference from DRAM refreshes

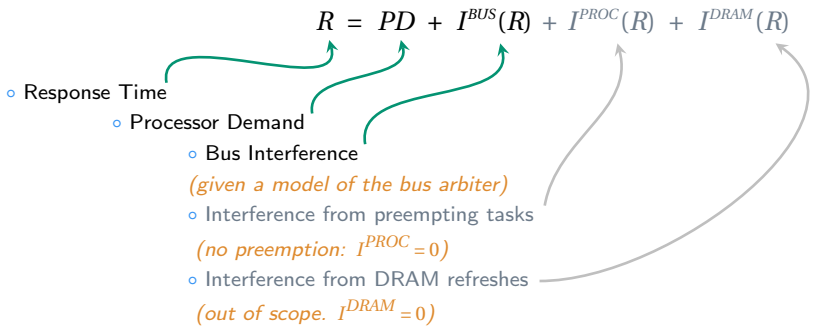
(out of scope. $I^{DRAM} = 0$)

Response Time Analysis



- Fix-point formula ⇒ iterative algorithm.

Response Time Analysis



- Fix-point formula ⇒ iterative algorithm.
- Multiple shared resources (memory banks)

Response Time Analysis

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$$I^{BUS}(R) = \sum_{b \in B} I_b^{BUS}(R)$$

where B: a set of memory banks

Response Time Analysis

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$$I^{BUS}(R) = \sum_{b \in B} I_b^{BUS}(R)$$

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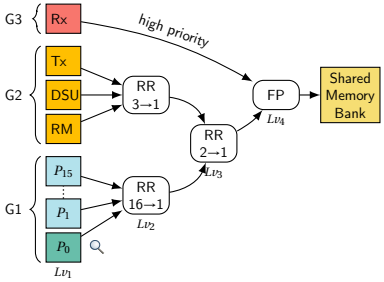
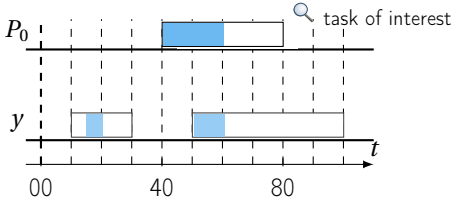
🔍 Requires a model of the bus arbiter

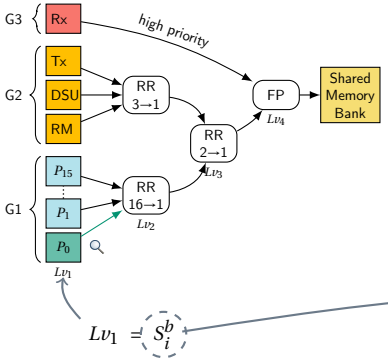
Model of the MPPA Bus



I_b^{BUS}: delay from all accesses + concurrent ones



Model of the MPPA Bus



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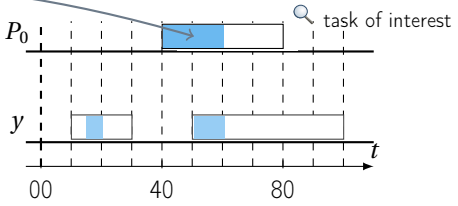

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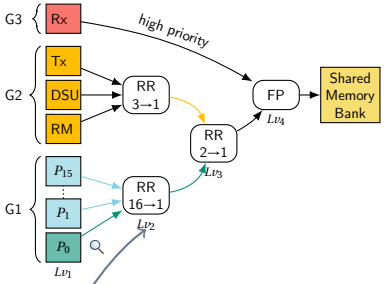

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$$Lv_1 = S_i^b$$

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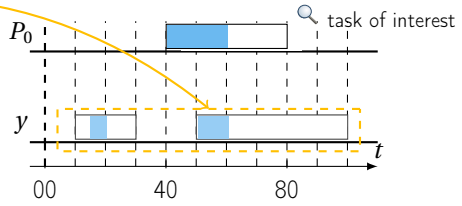
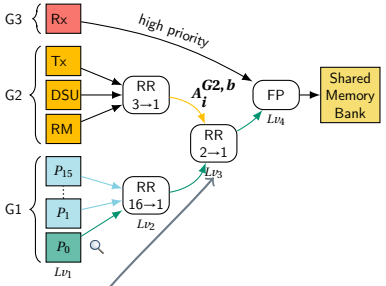


Model of the MPPA Bus



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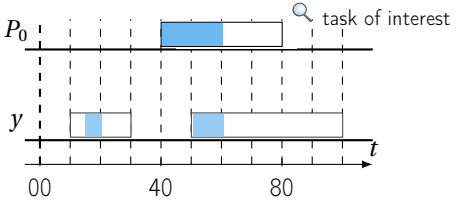

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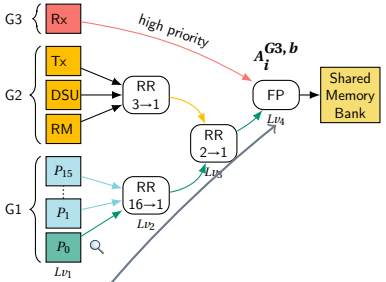

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$$Lv_4 = Lv_4 + A_i^{G3,b}$$

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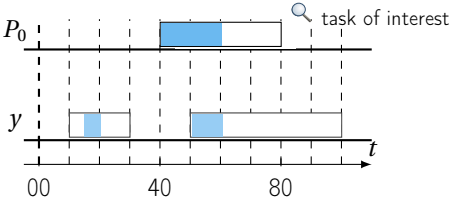

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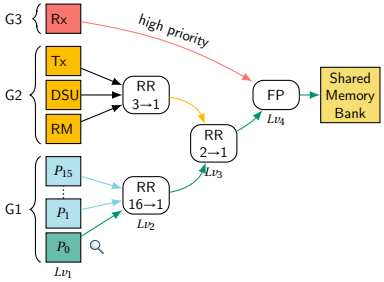

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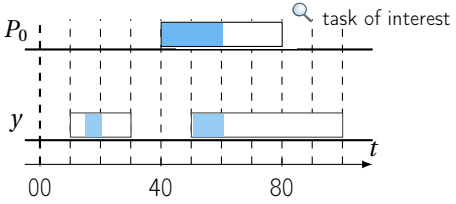
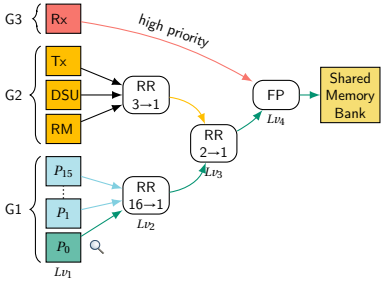


$$I_b^{BUS} = Lv_4 \times \text{Bus Delay}$$

Model of the MPPA Bus



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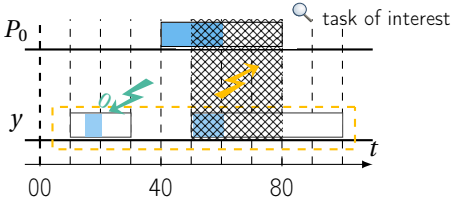
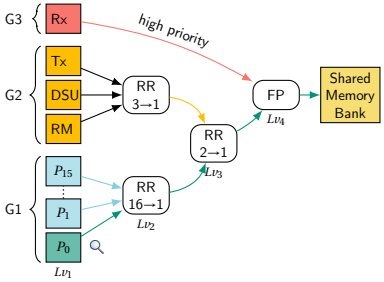


$I_b^{BUS} = Lv_4 \times$ Bus Delay

Model of the MPPA Bus



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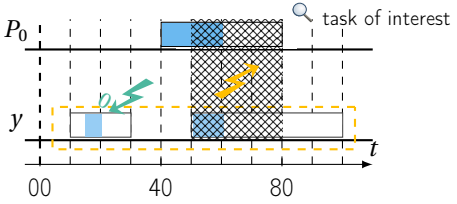
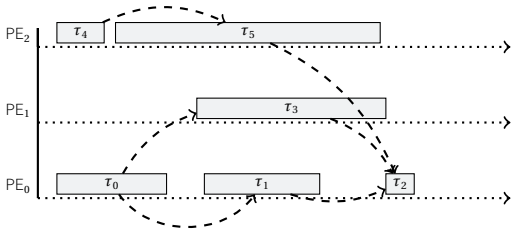


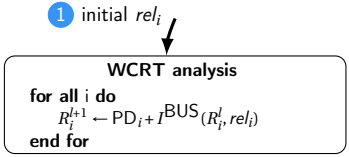
⚠ $A_i^{y,b}$ depends on rel_i and R_i

$I_b^{BUS} = Lv_4 \times$ Bus Delay

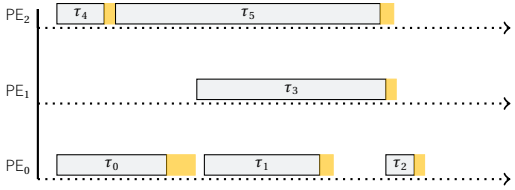
Response Time Analysis with Dependencies

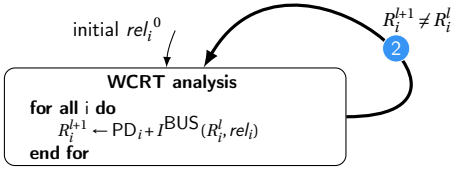


1 Start with initial release dates.



Response Time Analysis with Dependencies

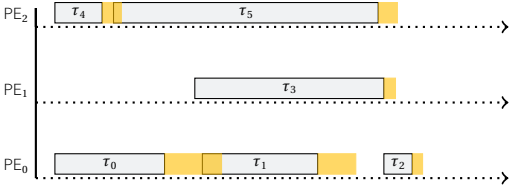


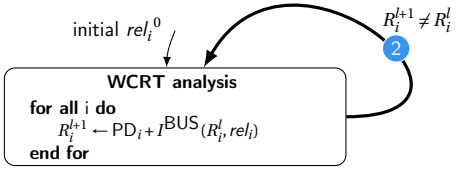


1. Start with initial release dates.
2. Compute response times

...

Response Time Analysis with Dependencies





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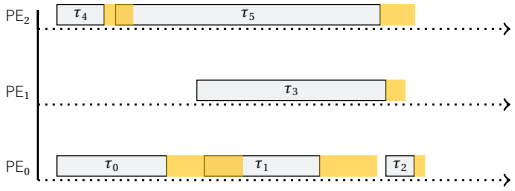
Response Time Analysis with Dependencies



1. Start with initial release dates.
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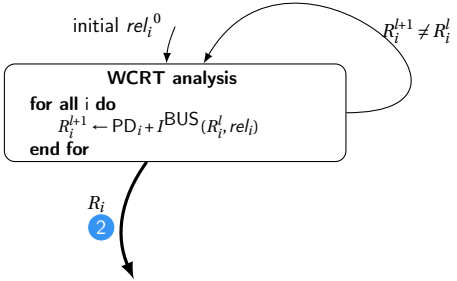
   ... ... a fixed-point is reached!



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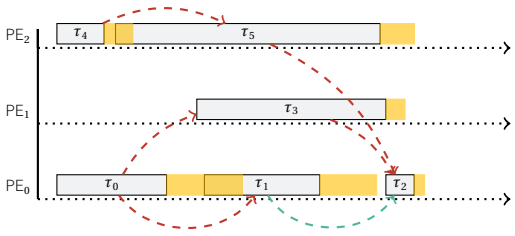

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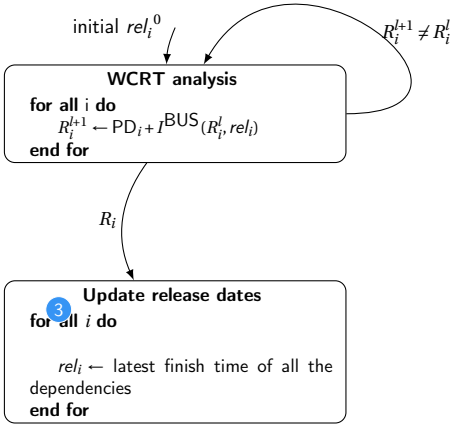

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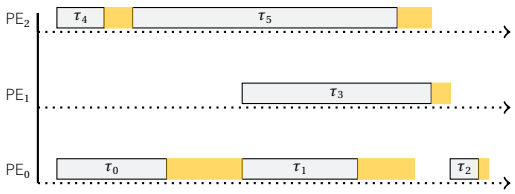

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4. Repeat until no release date changes
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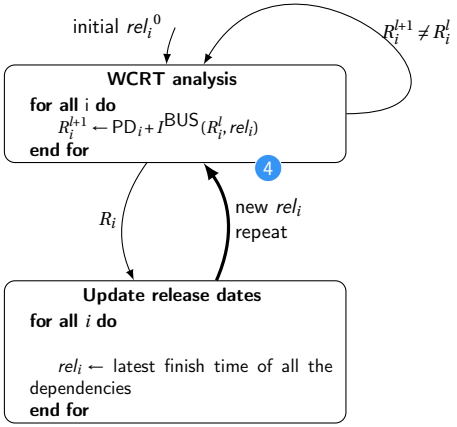
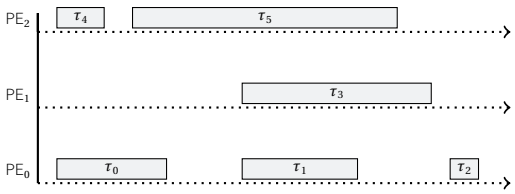


Response Time Analysis with Dependencies



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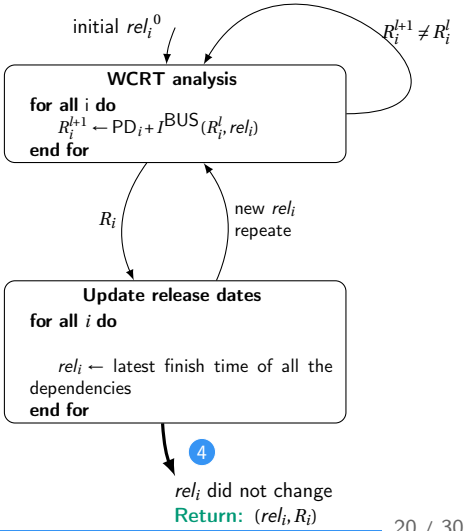
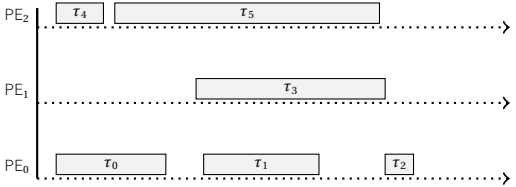
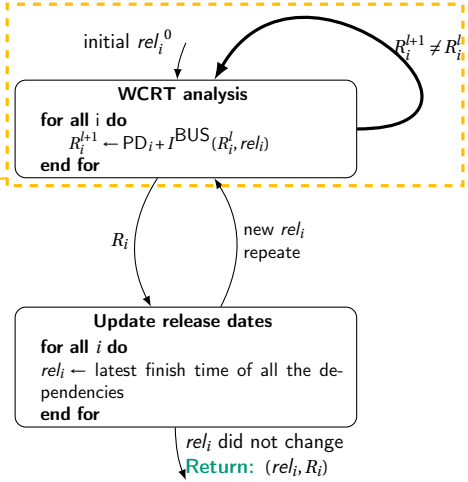


Proof of Convergence Toward a Fixed-point



- Convergence of the 1^{st} fixed-point iteration:



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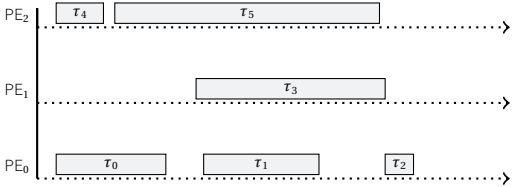
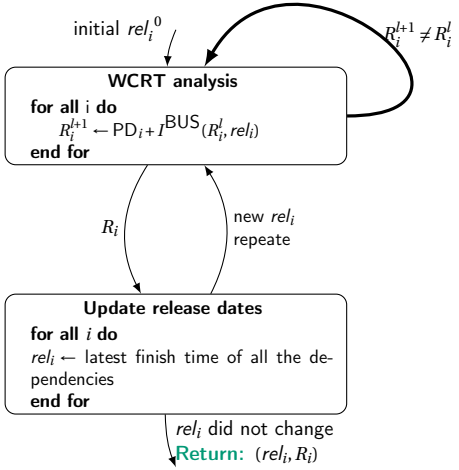


- Convergence of the 1^{st} fixed-point iteration:
  - Monotonic and bounded ✓



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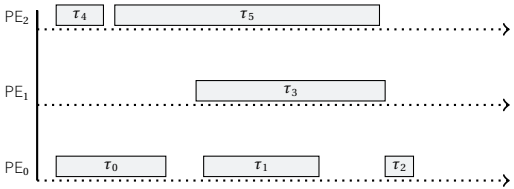

- Convergence of the 1^{st} fixed-point iteration:
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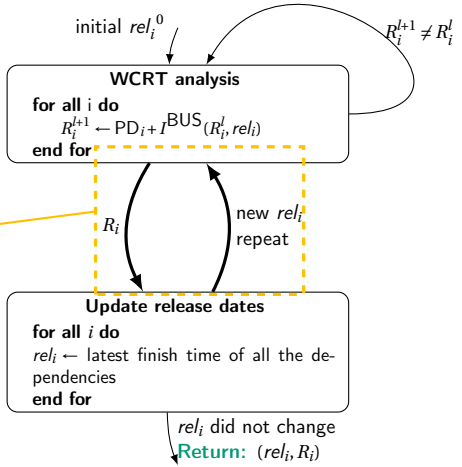

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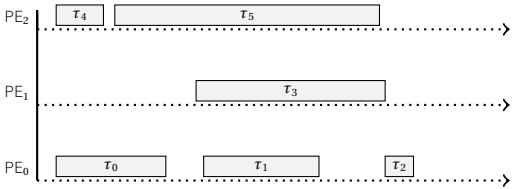

- Convergence of the 1^{st} fixed-point iteration:
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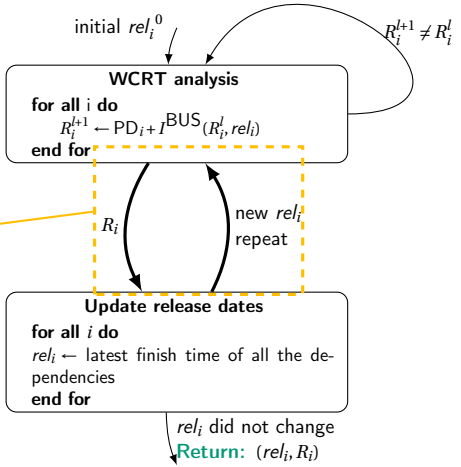
- Convergence of the 2^{nd} fixed-point iteration:
  - no monotonicity: R_i and rel_i may grow or shrink at each iteration. ?



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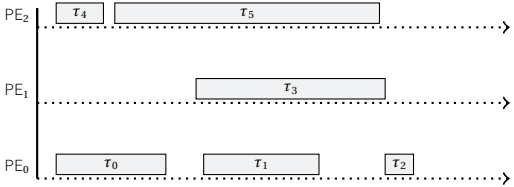

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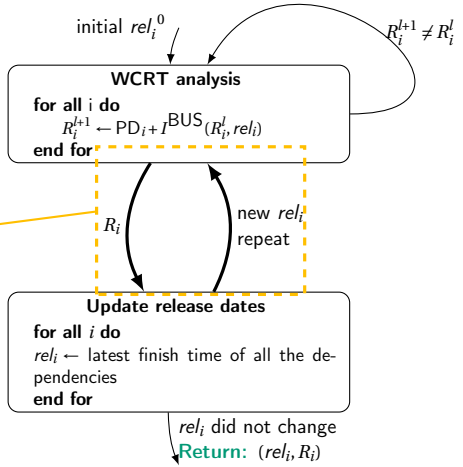
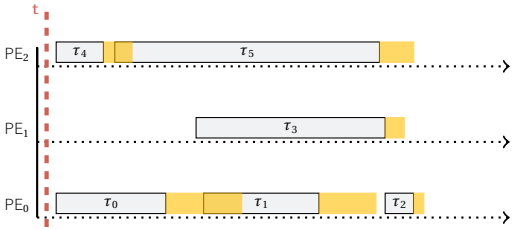


Theorem

At each iteration, at least one task finds its final release date.

Full proof in our technical report:
http://www-verimag.imag.fr/TR/TR-2016-1.pdf

Proof of Convergence Toward a Fixed-point



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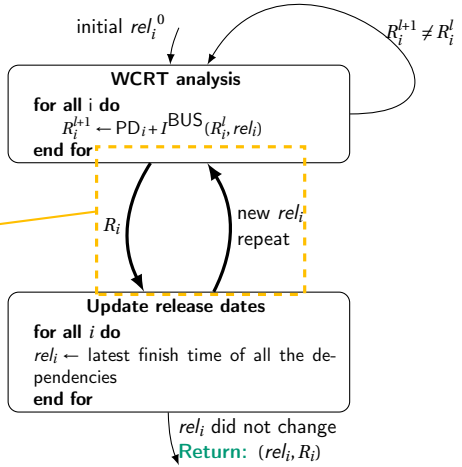

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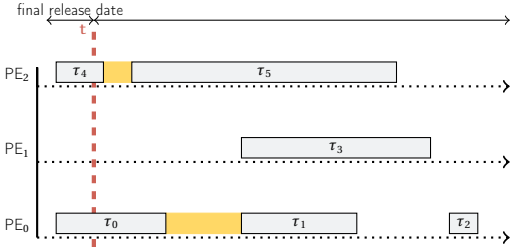

- Convergence of the 1^{st} fixed-point iteration:
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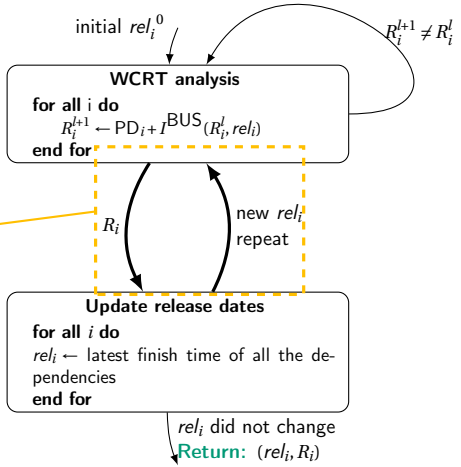

Theorem

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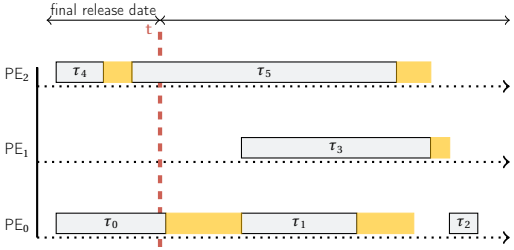

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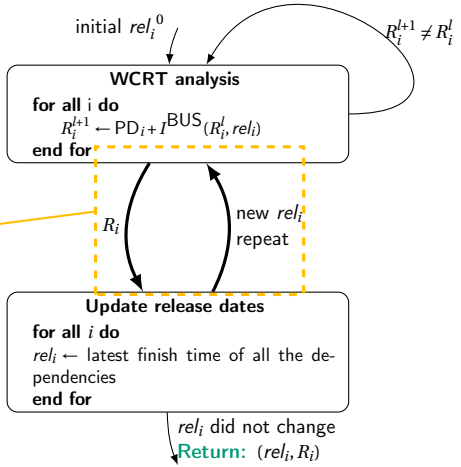

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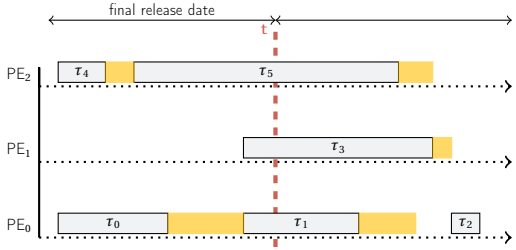

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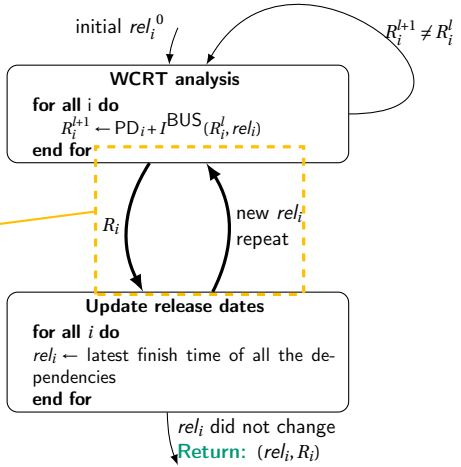

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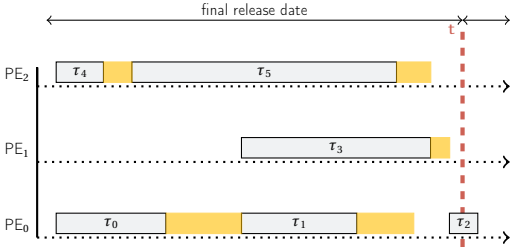

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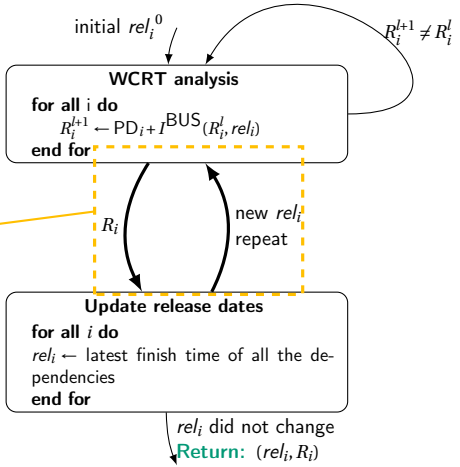

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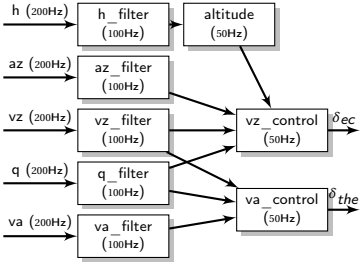
Outline

Evaluation: ROSACE Case Study[1]



- Flight management system controller

[1] Pagetti et al., RTAS 2014

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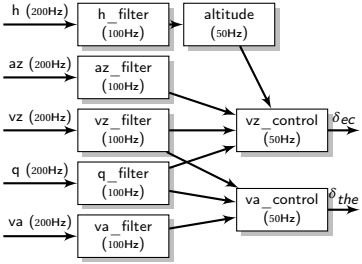

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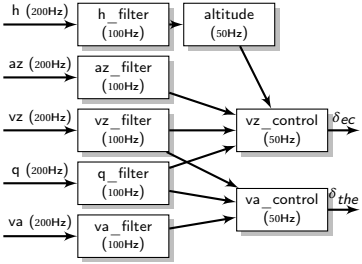

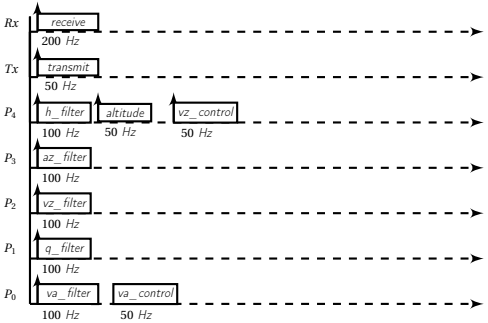

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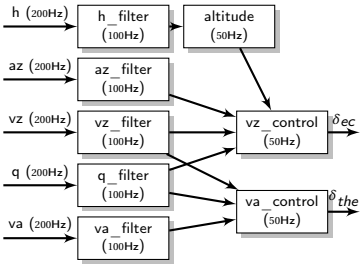

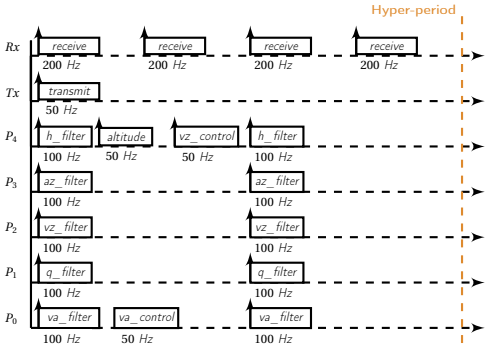

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Task	Processor Demand (cycles)	Memory Demand (accesses)
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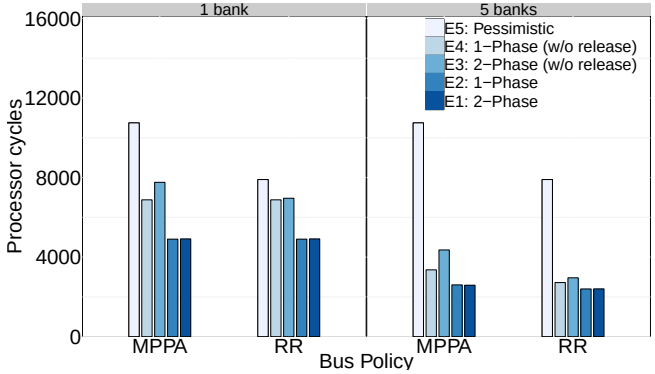
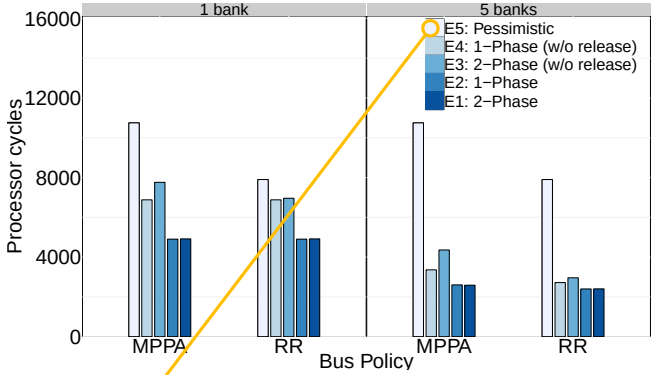
Experiments: Find the smallest schedulable hyper-period

Evaluation: Experiments



Smallest schedulable hyper-period

Evaluation: Experiments



E5: All accesses interfere

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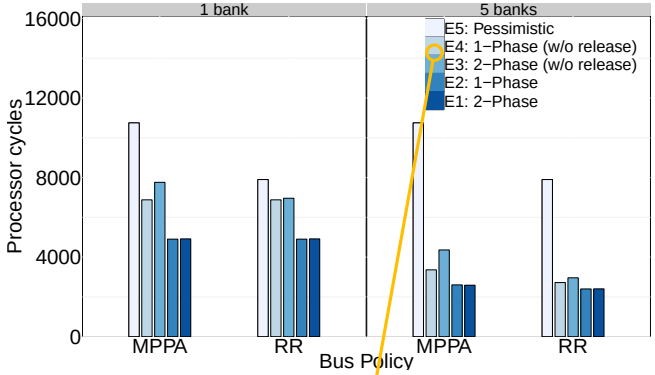

Smallest schedulable hyper-period

E4, E3: We don't use the release dates

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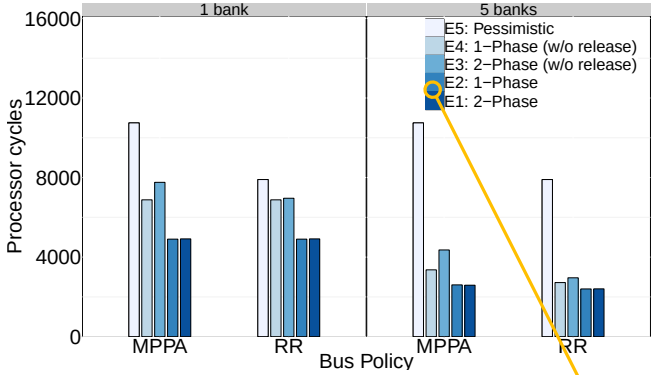

Smallest schedulable hyper-period

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E2, E1: Our approach. We use the release dates

Evaluation: Experiments

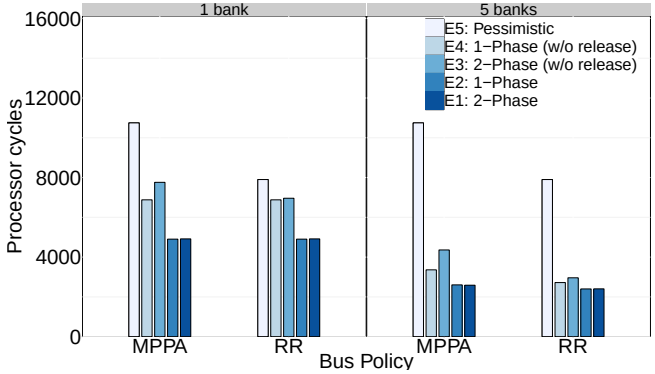
1-Phase model

memory access pattern 

2-Phase model

memory access pattern 

- Phases are modeled as sub-tasks



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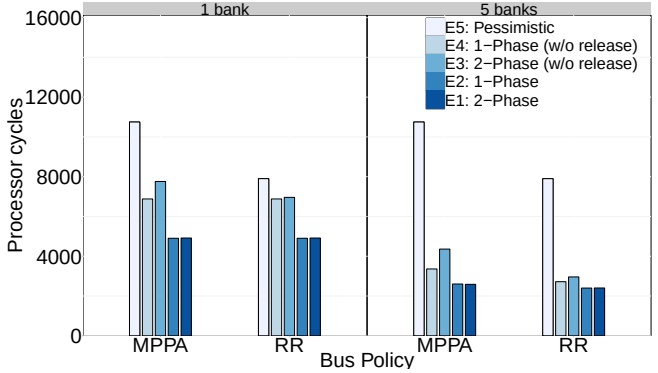
Taking into account the memory banks improves the analysis with a factor in $[1.77, 2.52]$



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Speedup factors

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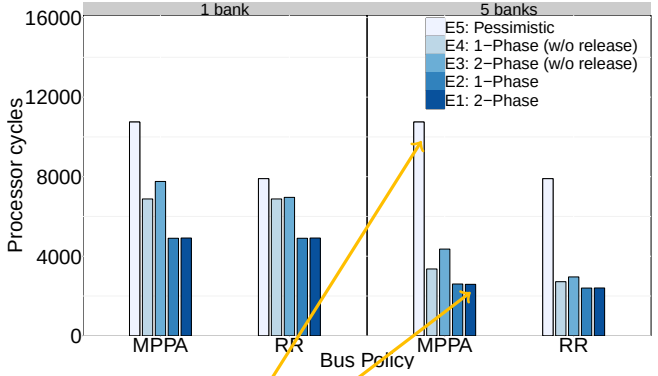

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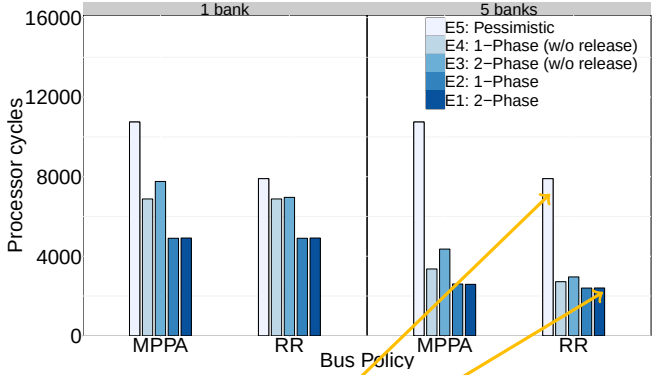

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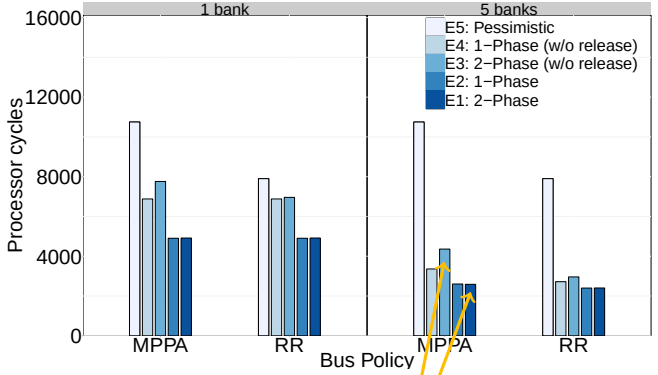

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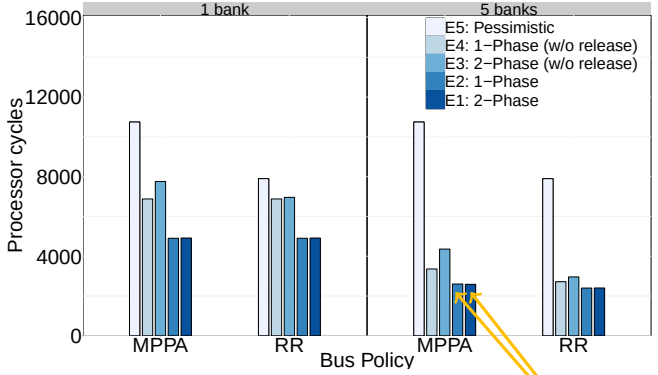

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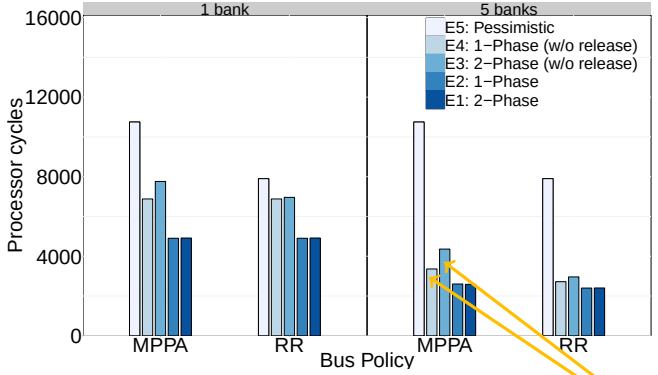

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Speedup factors

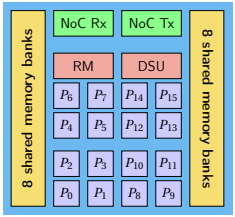
Outline

Conclusion

- Code generation and real-time analysis for many-core (Kalray MPPA 256)
  = major challenge for industry and research
- Hard Real-Time ⇒ simplicity, predictability ⇒ static, time-driven schedule
- Critical ⇒ traceability ⇒ no aggressive optimization
- Our work:
  - Understand and model the precise architecture of MPPA
  - Extension of Multi-Core Response Time Analysis
  - Non-trivial proof of termination

Future Work

- Model of the Resource Manager.



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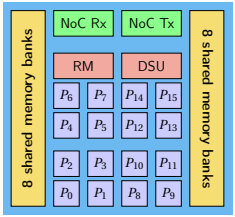

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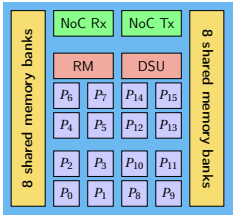

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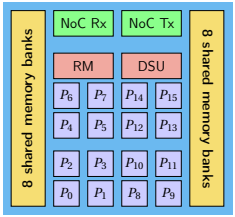

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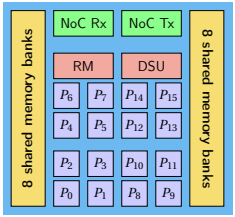

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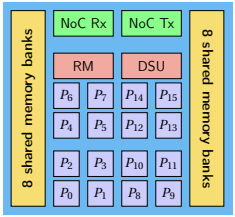

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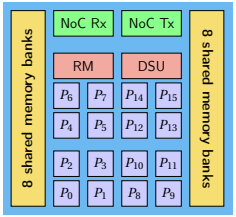

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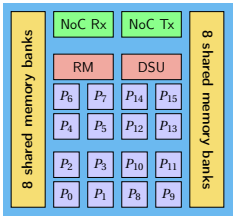

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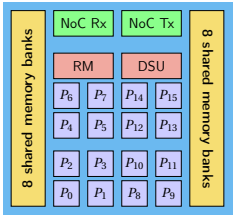

Questions?

Outline

Compilation and
Analysis for
Software and
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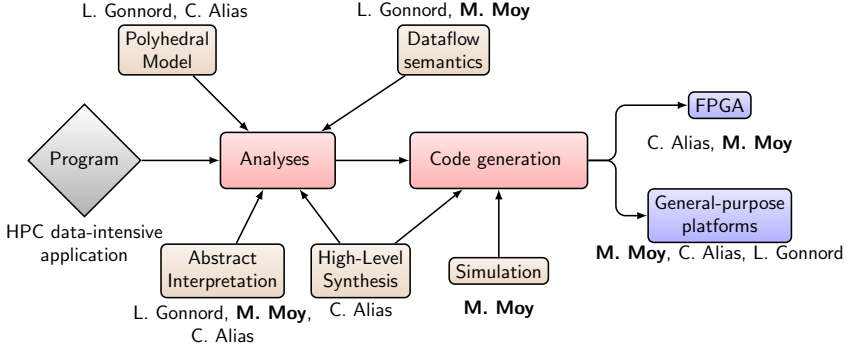
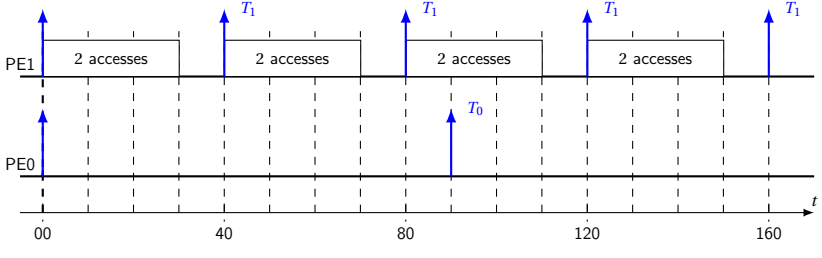


BACKUP

Multicore Response Time Analysis

Example: Fixed Priority bus arbiter, PE1 > PE0
Bus access delay = 10



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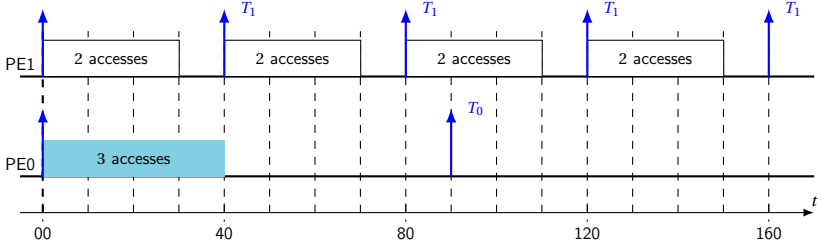

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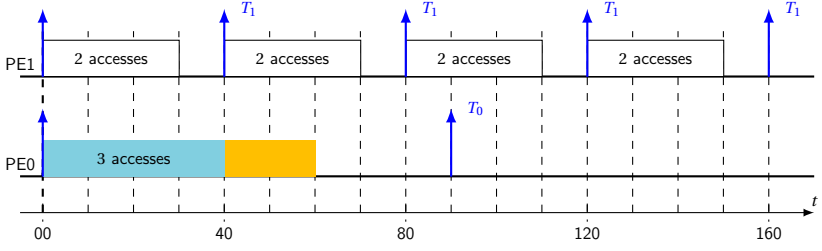

- Task of interest running on $PE0$:

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  $R_1 = 10 + 3 \times 10 + 2 \times 10 = 60$

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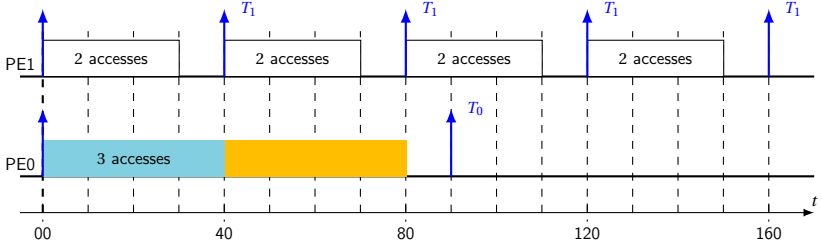
Example: Fixed Priority bus arbiter, PE1 > PE0
Bus access delay = 10



- Task of interest running on $PE0$:

  $R_0 = 10 + 3 \times 10$ (response time in isolation)

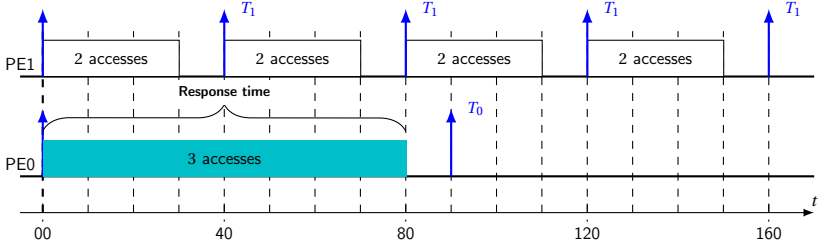
  $R_1 = 10 + 3 \times 10 + 2 \times 10 = 60$

  $R_2 = 10 + 3 \times 10 + 2 \times 10 + 2 \times 10 = 80$

[1] Altmeyer et al., RTNS 2015

Multicore Response Time Analysis

Example: Fixed Priority bus arbiter, PE1 > PE0
Bus access delay = 10



- Task of interest running on $PE0$:

  $R_0 = 10 + 3 \times 10$ (response time in isolation)

  $R_1 = 10 + 3 \times 10 + 2 \times 10 = 60$

  $R_2 = 10 + 3 \times 10 + 2 \times 10 + 2 \times 10 = 80$

  $R_3 = 10 + 3 \times 10 + 2 \times 10 + 2 \times 10 + 0 = 80$ (fixed-point)

[1] Altmeyer et al., RTNS 2015

The Global Picture